

CLAIMS

What is claimed is:

1. A compensation circuit for an amplifier including at least first and second amplifier stages, comprising:

a first capacitance having one end that communicates with an input of the first amplifier stage;

an amplifier having a first gain, an input that communicates with an opposite end of said first capacitance, and an output; and

a second capacitance having a first end that communicates with said output of said broadband amplifier and an opposite end that communicates with an input of the second amplifier stage.

2. The compensation circuit of Claim 1 wherein said amplifier is a broadband amplifier.

3. The compensation circuit of Claim 2 wherein said broadband amplifier includes:

a current source; and

a transimpedance amplifier having an output and an input that communicates with said current source.

4. The compensation circuit of Claim 3 wherein said current source includes:

a first transistor including a control terminal and first and second terminals;

a bias resistance having one end that communicates with said control terminal of said first transistor and an opposite end that communicates with said first terminal of said first transistor; and

a current source that communicates with said first terminal.

5. The compensation circuit of Claim 3 wherein said transimpedance amplifier includes:

a first transistor having a control terminal and first and second terminals;

a feedback resistance having one end that communicates with said control terminal and an opposite end that communicates with said first terminal; and

a current source that communicates with said first terminal.

6. The compensation circuit of Claim 1 further comprising a broadband buffer having an input that communicates with said output of said amplifier and an output that communicates with said one end of said second capacitance.

7. The compensation circuit of Claim 6 wherein said broadband buffer includes:

a first transistor having a control terminal and first and second terminals;

a second transistor having a control terminal, a first terminal that communicates with said second terminal of said first transistor, and a second terminal;

third, fourth, and fifth transistors each having a control terminal and first and second terminals, wherein said control terminal of said third transistor communicates with said control terminal of said second transistor, said first terminal of said third transistor communicates with said control terminal of said fourth transistor, said first terminal of said fourth transistor communicates with said control terminal of said fifth transistor, and said first terminal of said first transistor communicates with said first terminal of said fifth transistor;

a resistance having one end that communicates with said first terminal of said third transistor and an opposite end that communicates with said first terminal of said fourth transistor; and

a feedback capacitance having one end that communicates with said first terminal of said first transistor and an opposite end that communicates with said control terminals of said second and third transistors.

8. An amplifier circuit comprising the compensation circuit of Claim 6 and further comprising:

said first amplifier stage; and

said second amplifier stage.

9. The amplifier circuit of Claim 8 further comprising a load capacitance having one end that communicates with an output of said second amplifier stage.

10. The amplifier circuit of Claim 8 further comprising:
a first impedance that has one end that communicates with said input of said first amplifier stage; and

a second impedance that has one end that communicates with said input of said first amplifier stage and an opposite end that communicates with said output of said second amplifier stage.

11. The amplifier circuit of Claim 10 wherein said first impedance is at least one of a resistance, a capacitance and a short circuit.

12. The amplifier circuit of Claim 10 wherein said second impedance is at least one of a resistance, a capacitance and a short circuit.

13. A power supply, comprising:
- a first amplifier stage having an input and an output;
 - a second amplifier stage having an input that communicates with said output of said first amplifier stage and an output; and
 - a compensation circuit comprising:
 - a first capacitance having one end that communicates with said input of said first amplifier stage;
 - an amplifier having a first gain, an input that communicates with an opposite end of said first capacitance, and an output; and
 - a second capacitance having a first end that communicates with said output of said amplifier and an opposite end that communicates with said input of said second amplifier stage.

14. The power supply of Claim 13 wherein said amplifier is a broadband amplifier.

15. The power supply of Claim 14 wherein said broadband amplifier includes:

- a current source; and
- a transimpedance amplifier having an output and an input that communicates with said current source.

16. The power supply of Claim 15 wherein said current source includes:

a first transistor including a control terminal and first and second terminals;

a bias resistance having one end that communicates with said control terminal of said first transistor and an opposite end that communicates with said first terminal of said first transistor; and

a current source that communicates with said first terminal.

17. The power supply of Claim 15 wherein said transimpedance amplifier includes:

a first transistor having a control terminal and first and second terminals;

a feedback resistance having one end that communicates with said control terminal and an opposite end that communicates with said first terminal; and

a current source that communicates with said first terminal.

18. The power supply of Claim 13 further comprising a broadband buffer having an input that communicates with said output of said amplifier and an output that communicates with said one end of said second capacitance.

19. The power supply of Claim 16 wherein said broadband buffer includes:

a first transistor having a control terminal and first and second terminals;

a second transistor having a control terminal, a first terminal that communicates with said second terminal of said first transistor, and a second terminal;

third, fourth, and fifth transistors each having a control terminal and first and second terminals, wherein said control terminal of said third transistor communicates with said control terminal of said second transistor, said first terminal of said third transistor communicates with said control terminal of said fourth transistor, said first terminal of said fourth transistor communicates with said control terminal of said fifth transistor, and said first terminal of said first transistor communicates with said first terminal of said fifth transistor;

a resistance having one end that communicates with said first terminal of said third transistor and an opposite end that communicates with said first terminal of said fourth transistor; and

a feedback capacitance having one end that communicates with said first terminal of said first transistor and an opposite end that communicates with said control terminals of said second and third transistors.

20. The power supply of Claim 13 further comprising a load capacitance that communicates with an output of said second amplifier stage.

21. The power supply of Claim 13 further comprising:

a first impedance that has one end that communicates with said input of said first amplifier stage; and

a second impedance that has one end that communicates with said input of said first amplifier stage and an opposite end that communicates with said output of said second amplifier stage.

22. The power supply of Claim 21 wherein said first impedance is at least one of a resistance, a capacitance and a short circuit.

23. The power supply of Claim 21 wherein said second impedance is at least one of a resistance, a capacitance and a short circuit.

24. A broadband inverter, comprising:

a first transistor having a control terminal and first and second terminals;

a second transistor having a control terminal, a first terminal that communicates with said second terminal of said first transistor, and a second terminal;

third, fourth, and fifth transistors each having a control terminal and first and second terminals, wherein said control terminal of said third transistor communicates with said control terminal of said second transistor, said first terminal of said third transistor communicates with said control terminal of said fourth transistor, said first terminal of said fourth transistor communicates with said control terminal of said fifth transistor, and said first terminal of said first transistor communicates with said first terminal of said fifth transistor; and

a feedback capacitance having one end that communicates with said first terminal of said first transistor and an opposite end that communicates with said control terminals of said second and third transistors.

25. The broadband inverter of Claim 24 further comprising a resistance having one end that communicates with said first terminal of said third transistor and an opposite end that communicates with said first terminal of said fourth transistor.

26. The broadband inverter of Claim 24 wherein said first transistor is a PMOS transistor, said control terminal of said first transistor is a gate, said first terminal of said first transistor is a source and said second terminal of said first transistor is a drain.

27. The broadband inverter of Claim 24 wherein said second, third, fourth and fifth transistors are NMOS transistors, said control terminals of said second, third, fourth and fifth transistors are gates, said first terminals of said second, third, fourth and fifth transistors are sources and said second terminals of said second, third, fourth and fifth transistors are drains.

28. The broadband inverter of Claim 24 further comprising first, second, third, and fourth current sources that communicate with said first terminals of said first, third, fourth and fifth transistors, respectively.

29. The broadband inverter of Claim 24 wherein said control terminal of said first transistor receives an input voltage and an output voltage is produced at said first terminal of said fifth transistor.